WHAT IS CLAIMED IS:

1. A fast Fourier transform (FFT) operating apparatus to carry out a FFT operation in a programmable processor chip, comprising:

a program controller to generate a FFT start signal and control a programmable processor;

a program memory to store an application of the programmable processor;

an FFT address generator to remove a looping instruction used for the FFT and a cycle for an address generation, and generate an offset address of a butterfly input data and an operation stop signal;

an address generator to calculate an address of a data memory using the offset address generated in the FFT address generator;

a data memory to store a data;

a data processor to carry out an arithmetic and logic operation using the data stored in the data memory; and

a flag register to generate a FFT operation signal.

2. The apparatus of claim 1, wherein the FFT address generator comprises:

a logical sum logic to generate initialization signals of a register to store a loop count value and a register to store a group count value according to the start signal and a group count match signal;

a first adder to update a group offset with a value obtained by multiplying the group offset and a loop count max value by 2;

GR, WR, LCR, and GCR registers to store the group offset, a twiddle factor, the loop count max value, and a group count max value;

a group counter to calculate the group count value;

a loop counter to calculate the loop count value;

a glue logic having a logic which generates a signal to initialize the group counter and the loop counter;

a second adder to add the group offset and the loop count value and output a single input data address;

a third adder to input with and add the second adder and the loop count max value and output another input data address;

a first comparator to compare a value of the loop counter and the loop count max value;

a second comparator to compare a value of the group counter and the group count max value; and

a third comparator to input with a N value and the group count max value and compare the group count max value with a N/2 value.

3. The apparatus of claim 1, wherein the data processor comprises:

a data bus switch circuit to provide the butterfly input data from the data memory and write an output data in the data memory;

a butterfly operation circuit having two multiplier-accumulators to multiply and accumulate a data and one arithmetic and logic unit;

an exponential operation circuit to carry out an exponential operation of a data in the butterfly operation;

an input register to store a value of the data memory; and

an accumulator to store an operation result and re-use the stored value for the

operation.

4. A radix-2 complex fast Fourier transform (FFT) operation method to carry out a FFT operation in a programmable processor chip, comprising:

generating a start signal and applying a FFT operation signal if the FFT starts;

generating an offset address of a butterfly input/output data to read a data and write an operated result in a data memory;

storing the generated offset address of the butterfly input/output data in an offset register of a programmable processor;

switching a data to provide the butterfly input data from the data memory and write the output data in the data memory;

carrying out a butterfly operation using two multiplier-accumulators, an arithmetic and logic unit, and an exponenter; and

generating a stop signal and resetting the FFT operation signal when the operation is ended.

5. The method of claim 4, wherein operation instructions SBUTTERFLY and ABUTTERFLY are used for the FFT operation.

6. The method of claim 4, wherein generating the offset address by a FTT address generator comprises:

starting the FFT if the FFT start signal is '1';

initializing a group count, a loop count, and a group count max value to '1' ,respectively, a group offset value to '-1', a loop count max value to 'N/2', and an

offset address value of a twiddle factor to '0' if the FFT starts;

calculating an input data by adding the group offset and the loop count values and calculating another input data by adding the group offset, the loop count, and the loop count max values;

increasing the loop count value by 1 if the loop count value is not equal to the loop count max value and resuming from calculating the two input data addresses;

initializing the loop count value to '1', setting the group offset value with a value obtained by multiplying the loop count max value by 2 and adding the group offset value to the multiplied value, and increasing the twiddle factor value by 1 if the loop count value is equal to the loop count max value;

increasing the group count value by 1 and resuming from calculating the two input data addresses if the group count is not equal to the group count max value;

initializing the group count value to '1', the group offset value to '-1', and the twiddle factor value to '0', dividing the loop count max value by 2, and multiplying the group count max value by 2 if the group count value is equal to the group count max value;

generating the operation stop signal and ending the FFT operation if the group count max value is greater than N/2; and

resuming from calculating the two input data addresses if the group count max value is not greater than N/2.